This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-3 (canceled)

Claim 4 (currently amended): ~~The phase detector according to claim 3~~ A phase detector configured to output an up signal when a first clock signal is ahead of a second clock signal in phase, and outputting a down signal when said first clock signal is behind said second clock signal in phase, said phase detector comprising:

first, second and third flip-flops;

~~wherein said~~ an F/F control circuit which brings said first flip-flop to ~~the~~ a reset state when at least one of said first and second clock signals has a first logic, brings said first flip-flop to ~~the~~ a set state when both said second and third flip-flops are in the set state, brings said second flip-flop to the set state when said first clock signal has a second logic and said first flip-flop is in the reset state, brings said second flip-flop to the reset state when both said second and third flip-flops are in the set state, brings said third flip-flop to the set state when said second clock signal has the second logic and said first flip-flop is in the reset state, and brings said third flip-flop to the reset state when both said second and third flip-flops are in the set state; and

an up/down signal output circuit configured to output said up signal and the down signal based on the outputs of said second and third flip-flops.

Claim 5 (original): The phase detector according to claim 4 wherein said F/F control circuit comprises:

a first logic circuit configured to reset said first flip-flop when at least one of said first and second clock signals has said first logic;

a second logic circuit configured to bring said second flip-flop to the set state when said first flip-flop is in the reset state and said first clock signal has said second logic;

a third logic circuit configured to bring said third flip-flop to the set state when said first flip-flop is in the reset state and said second clock signal has said second logic;

a fourth logic circuit configured to bring said second and third flip-flops to the reset state when both said second and third flip-flops are in the set state;

a fifth logic circuit configured to output said up signal when said second flip-flop is in the set state and said third flip-flop is in the reset state; and

a sixth logic circuit configured to output said down signal when said third flip-flop is in the set state and said second flip-flop is in the reset state.

Claim 6 (original): The phase detector according to claim 5 wherein said first flip-flop is brought to the reset state when an output of said first logic circuit has the first logic, and brought to the set state when the output of said fourth logic circuit has said first logic;

said second flip-flop is brought to the set state when the output of said second logic circuit has said first logic, and brought to the reset state when the output of said fourth logic circuit has said first logic, and

said third flip-flop is brought to the set state when the output of said third logic circuit has said first logic, and brought to the reset state when the output of said fourth logic circuit has said first logic.

Claim 7 (original): The phase detector according to claim 6 wherein each of said first, second and third flip-flops comprises a set input terminal, a reset input terminal, and first and second NAND gates,

said first NAND gate performs a NAND operation between the set input terminal and an output terminal of said second NAND gate,

said second NAND gate performs the NAND operation between the reset input terminal and the output terminal of said first NAND gate, and

the output of said first NAND gate forms respective outputs of said corresponding first, second and third flip-flops.

Claim 8 (original): The phase detector according to claim 6 wherein said first logic is a high level, and said second logic is a low level.

Claim 9 (original): The phase detector according to claim 5 wherein said first flip-flop is brought to the reset state when an output of said first logic circuit has said second logic, and brought to the set state when the output of said fourth logic circuit has said second logic;

said second flip-flop is brought to the set state when the output of said second logic circuit has said second logic, and brought to the reset state when the output of said fourth logic circuit has said second logic, and

said third flip-flop is brought to the set state when the output of said third logic circuit has said second logic, and brought to the reset state when the output of said fourth logic circuit has said second logic.

Claim 10 (original): The phase detector according to claim 9 wherein each of said first, second and third flip-flops comprises a set input terminal, a reset input terminal, first and second NOR gates, and an inverter,

said first NOR gate performs a NOR operation between the set input terminal and an output terminal of said second NOR gate,

said second NOR gate performs the NOR operation between the reset input terminal and the output terminal of said first NOR gate,

said inverter reverses an output of said first NOR gate, and

the output of said inverter forms respective outputs of said corresponding first, second and third flip-flops.

Claim 11 (original): The phase detector according to claim 9 wherein said first logic is a high level, and said second logic is a low level.

Claims 12-14 (canceled)

Claim 15 (currently amended): ~~The phase locked loop circuit according to claim 12 wherein~~ A phase locked loop circuit comprising:

a charge pump configured to output a voltage signal in accordance with an up signal and a down signal;

a loop filter configured to remove a high frequency component included in an output of said charge pump;

a voltage control oscillation circuit configured to output a signal of a frequency in accordance with an output voltage of said loop filter;

a clock buffer configured to output a clock signal in accordance with an output of said voltage control oscillation circuit; and

a phase detector configured to output the up signal when a fist clock signal is ahead of a second clock signal in phase, and outputting a down signal when said first clock signal is behind said second clock signal in phase,

wherein said phase detector comprises:

first, second and third flip-flops;

~~said~~ an F/F control circuit which brings said first flip-flop to a reset state when at least one of said first and second clock signals has a first logic, brings said first flip-flop to a set state when both said second and third flip-flops are in the set state, brings said second flip-flop to the set state when said first clock signal has a second logic and said first flip-flop is in the reset state, brings said second flip-flop to the reset state when both said second and third flip-flops are in the set state, brings said third flip-flop to the set state when said second clock signal has the second logic and said first flip-flop is in the reset state, and brings said third flip-flop to the reset state when both said second and third flip-flops are in the set state; and

an up/down signal output circuit configured to output the up signal and the down signal based on the outputs of said second and third flip-flops.

Claim 16 (original): The phase locked loop circuit according to claim 15 wherein said F/F control circuit comprises:

a first logic circuit configured to reset said first flip-flop when at least one of said first and second clock signals has said first logic;

a second logic circuit configured to bring said second flip-flop to the set state when said first flip-flop is in the reset state and said first clock signal has said second logic;

a third logic circuit configured to bring said third flip-flop to the set state when said first flip-flop is in the reset state and said second clock signal has said second logic;

a fourth logic circuit configured to bring said second and third flip-flops to the reset state when both said second and third flip-flops are in the set state;

a fifth logic circuit configured to output said up signal when said second flip-flop is in the set state and said third flip-flop is in the reset state; and

a sixth logic circuit configured to output said down signal when said third flip-flop is in the set state and said second flip-flop is in the reset state.

Claim 17 (original): The phase locked loop circuit according to claim 16 wherein said first flip-flop is brought to the reset state when an output of said first logic circuit has the first logic, and brought to the set state when the output of said fourth logic circuit has said first logic;

said second flip-flop is brought to the set state when the output of said second logic circuit has said first logic, and brought to the reset state when the output of said fourth logic circuit has said first logic, and

said third flip-flop is brought to the set state when the output of said third logic circuit has said first logic, and brought to the reset state when the output of said fourth logic circuit has said first logic.

Claim 18 (original): The phase locked loop circuit according to claim 17 wherein each of said first, second and third flip-flops comprises a set input terminal, a reset input terminal, and first and second NAND gates,

said first NAND gate performs a NAND operation between the set input terminal and an output terminal of said second NAND gate,

said second NAND gate performs the NAND operation between the reset input terminal and the output terminal of said first NAND gate, and

the output of said first NAND gate forms respective outputs of said corresponding first, second and third flip-flops.

Claim 19 (original): The phase locked loop circuit according to claim 16 wherein said first flip-flop is brought to the reset state when an output of said first logic circuit has said second logic, and brought to the set state when the output of said fourth logic circuit has said second logic;

said second flip-flop is brought to the set state when the output of said second logic circuit has said second logic, and brought to the reset state when the output of said fourth logic circuit has said second logic, and

said third flip-flop is brought to the set state when the output of said third logic circuit has said second logic, and brought to the reset state when the output of said fourth logic circuit has said second logic.

Claim 20 (original): The phase locked loop circuit according to claim 19 wherein each of said first, second and third flip-flops comprises a set input terminal, a reset input terminal, first and second NOR gates, and an inverter,

said first NOR gate performs a NOR operation between the set input terminal and an output terminal of said second NOR gate,

said second NOR gate performs the NOR operation between the reset input terminal and the output terminal of said first NOR gate,

said inverter reverses an output of said first NOR gate, and

the output of said inverter forms respective outputs of said corresponding first, second and third flip-flops.